IN THE CLAIMS:

Claims 31 - 32 and 34 - 35 have been amended.

Claim 1 - 26 (cancelled).

27. (previously presented) An input protection circuit comprising:

an input terminal for supplying an input signal to a circuit to be protected;

a semiconductor substrate of a first conductivity type;

a first well region of a second conductivity type opposite to the first conductivity type, said first well region being formed in one principal surface area of said semiconductor substrate and forming a PN junction with said semiconductor substrate;

first and second impurity doped regions of the first conductivity type formed in said first well region and forming a first lateral bipolar transistor with a portion of said first well region serving as a base;

a second well region of the first conductivity type formed in the principal surface area of said semiconductor substrate; and

third and fourth well regions of the second conductivity type formed in said second well region and forming a second lateral bipolar transistor with a portion of said second well region serving as a base, bottoms of said third and fourth well regions forming a PN junction with said second well or with said semiconductor substrate and the third well region being formed entirely inside the second well region;

wherein said input terminal is connected to said first impurity doped region, said second impurity doped region and the base of said first lateral bipolar transistor are connected to said third well region, said first lateral bipolar transistor operating without a fixed base bias, and said fourth well region and the base of the second lateral bipolar transistor are connected to one

reference potential node.

Claim 28 (cancelled).

29. (previously presented) An input protection circuit comprising:

an input terminal for supplying an input signal to a circuit to be protected;

a semiconductor substrate of a first conductivity type;

a first well region of a second conductivity type opposite to the first conductivity type, said first well region being formed in one principal surface area of said semiconductor substrate and forming a PN junction with said semiconductor substrate;

first and second impurity doped regions of the first conductivity type formed in said first well region and forming a first lateral bipolar transistor with a portion of said first well region serving as a base;

a second well region of the first conductivity type formed in the principal surface area of said semiconductor substrate; and

third and fourth well regions of the second conductivity type formed in said second well region and forming a second lateral bipolar transistor with a portion of said second well region serving as a base, bottoms of said third and fourth well regions forming a PN junction with said second well or with said semiconductor substrate and

the third and fourth well regions not being part of a MOS transistor,

wherein said input terminal is connected to said first impurity doped region, said second impurity doped region and the base of said first lateral bipolar transistor are connected to said third well region, said first lateral bipolar transistor operating without a fixed base bias, and said fourth well region and the base of the second lateral bipolar transistor are connected to one reference potential node.

30. (previously presented) An input protection circuit according to claim 27, further including a current limiting resistor formed on an insulating layer formed in the principal surface area of said semiconductor substrate, wherein said input terminal is connected via said current limiting resistor to said first impurity doped region.

31. (currently amended) The input protection circuit of claim 27, wherein the second lateral bipolar transistor is turned on to protect the ~~input protection~~ circuit to be protected when a high positive bias voltage is applied to the input terminal.

32. (currently amended) The input protection circuit of claim 27, wherein the first lateral bipolar transistor is turned on to protect the ~~input protection~~ circuit to be protected when a high negative bias voltage is applied to the input terminal.

33. (previously presented) An input protection circuit according to claim 29, further including a current limiting resistor formed on an insulating layer formed in the principal surface area of said semiconductor substrate, wherein said input terminal is connected via said current limiting resistor to said first impurity doped region.

34. (currently amended) The input protection circuit of claim 29, wherein the second lateral bipolar transistor is turned on to protect the ~~input protection~~ circuit to be protected when a high positive bias voltage is applied to the input terminal.

35. (currently amended) The input protection circuit of claim 29, wherein the first lateral bipolar transistor is turned on to protect the ~~input protection~~ circuit to be protected when a high negative bias voltage is applied to the input terminal.

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